Mol. Cryst. Liq. Cryst., Vol. 532: pp. 119/[535]–126/[542], 2010

ISSN: 1542-1406 print/1563-5287 online
DOI: 10.1080/15421406.2010.497055

Taylor & Francis
Taylor & Francis Group

Characterization of a-Si:H TFTs with Various Phosphorus Concentrations in a-SiN:H Layer

JUN-WOO KIM,[1] BYUNG-JU KIM,[1]
YOUNG-SOO SOHN,[2] AND SIE-YOUNG CHOI[1]

[1]School of Electrical Engineering & Computer Science,
Kyungpook National University, Daegu, Republic of Korea
[2]Catholic University of Daegu, Gyeongsan-si, Gyeongbuk,
Republic of Korea

Characteristics of hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) with various phosphorus doping concentrations in a-SiN:H layer have been investigated. The a-Si:H TFTs with a heterostructure of the phosphorus-contained a-SiN:H and intrinsic a-Si:H layers have been fabricated by a plasma enhanced chemical vapor deposition using SiH_4, PH_3, and NH_3 gases. The mobility, the threshold and the surface roughness of the devices have been investigated and compared with the conventional amorphous silicon thin film transistors.

Keywords a-Si:H TFT; a-SiN:H; mobility; phosphorus doping

Introduction

A hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) has been of extensive interest for the application as switching devices to large-area liquid crystal display (LCD) panels [1]. SiNx films deposited by a radio-frequency plasma enhanced chemical vapor deposition (RF-PECVD) are widely used as a protection layer of a gate metal. The performance and reliability of the a-Si:H TFT using the SiNx films as the gate dielectric layer are mainly governed by its chemical composition, surface roughness and internal stress which are strongly dependent on the deposition conditions [2,3].

Today the most popular structure for a-Si:H TFTs is the inverted staggered structure as shown in Figure 1. The semiconductor layer consists of an active layer (intrinsic a-Si:H) and an ohmic layer (n^+ a-Si:H). The commonly used gate insulator is the hydrogenated amorphous silicon nitride (a-SiN:H). The inverted staggered a-Si:H TFT operates in the accumulation mode. When a positive voltage is applied to the gate electrode, the band bending at or near the gate insulator/amorphous semiconductor interface is increased and electrons are accumulated near the interface

Address correspondence to Prof. Sie-Young Choi, School of Electrical Engineering & Computer Science, Kyungpook National University, 1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Republic of Korea. Tel.: (+82)53-950-5518; Fax: (+82)53-950-6837; E-mail: sychoi@ee.knu.ac.kr

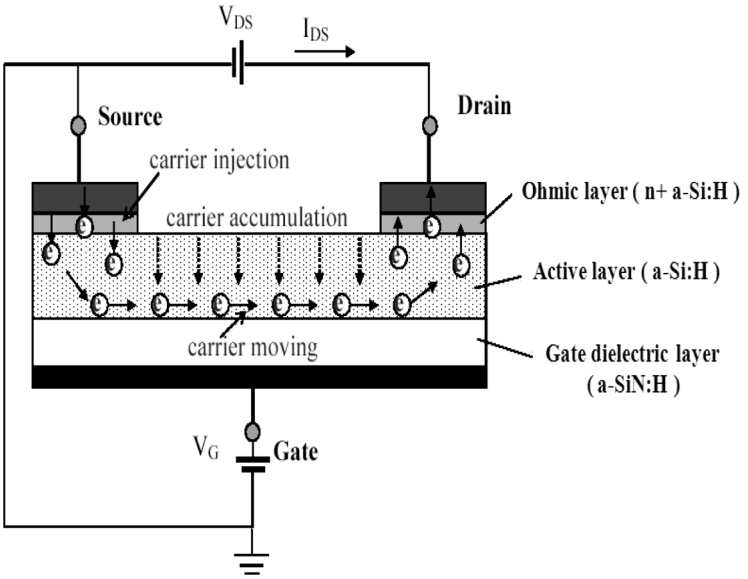

Figure 1. A schematic diagram of the inverted staggered a-Si:H TFT.

to form the conduction channel. If a positive drain voltage is applied to the drain electrode, the drain-source current flows from the drain to the source electrode through the n^+ a-Si:H and intrinsic a-Si:H (conduction channel) layers [4].

According to the theory of the a-Si:H TFT, the mobility of electrons depends on the carrier concentration in the channel. The conductivity can be increased with the doping concentration in the channel. However, increasing the doping concentration over some critical amount causes ion scattering by the impurities which leads to a degradation of the mobility. Therefore, improvement of the mobility focused on the appropriate phosphorus doping concentration in the a-SiN:H layer near the heterojunction [5]. This paper investigated the electron mobility of the a-Si:H TFTs as a function of the phosphorus doping concentration in the a-SiN:H layer.

Experimental

Bottom-gate a-Si:H TFTs with a back channel etch (BCE) structure were fabricated on glass substrates. Figure 2 shows the process flow of the inverted staggered a-Si:H TFT. A NiCr metal layer was deposited on a Corning 1737 glass by the thermal radio frequency method and defined for a gate electrode. SiN_x, a-Si:H and n^+ a-Si:H layers were deposited on the glass substrate subsequently using 13.56 MHz PECVD at 250°C without breaking the vacuum. The working pressure was 700 mTorr. The SiN_x layer was deposited using a gas mixture of SiH_4 and NH_3, the a-Si:H layer using H_2 and SiH_4, and the n^+ a-Si:H layer using SiH_4 and PH_3, respectively. The thickness of the SiN_x, a-Si:H and n^+ a-Si:H layers was 2,500 Å, 2,000 Å and 500 Å, respectively. Tables 1 and 2 indicate deposition conditions and etching conditions of the thin films. An active island was formed by dry etching. Al metal was deposited and defined to form the source/drain electrodes. Finally, the n^+ layer region between the source and drain electrodes was etched away.

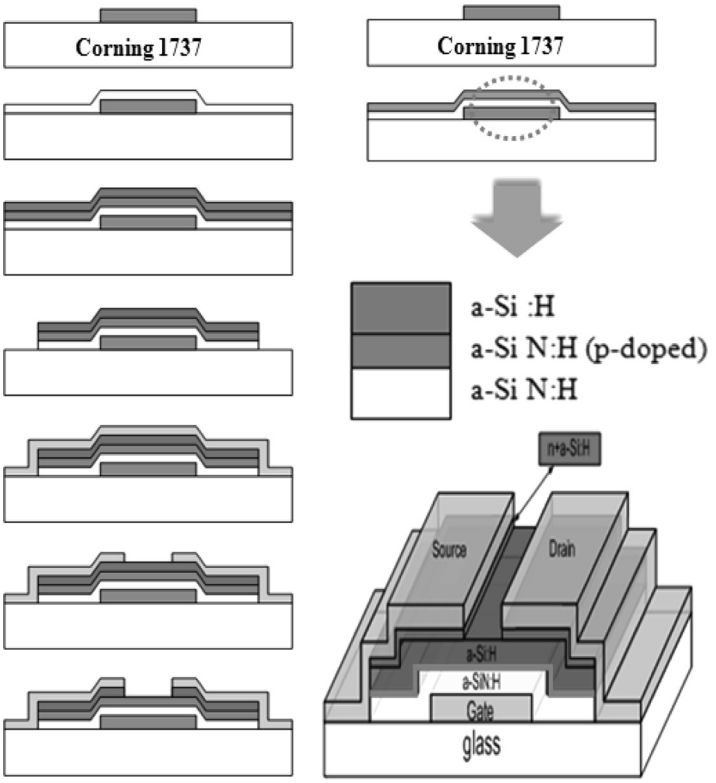

Figure 2. Process flow of the inverted staggered a-Si:H TFT.

One major key area is the various phosphorus doped a-SiN:H layer at the interface between the a-Si:H and the a-SiN:H. Thickness of the phosphorus doped a-SiN:H layer was fixed to 100 Å.

HP-4280A was used to measure the capacitance of the a-SiN:H thin film. Alpha-Step was used to measure the deposition rates of the various phosphorus

Table 1. Deposition conditions of a-SiN:H, a-Si:H, n^+ a-Si:H thin films

Parameter	a-SiN:H	a-Si:H	n^+ a-Si:H	Delta doping layer
Gas	SiH_4 (+89.5%He)/ NH_3	SiH_4 (+89.5%He)/ H_2	SiH_4 (+89.5%He)/ PH_3(+99%H_2)	SiH_4 (+89.5%He)/ NH_3/PH_3
Flow rate (sccm)	30/45	20/18	20/50	30/45/0∼18
r.f. power (W)	200	150	100	200
Substrate temperature (°C)	250	250	250	250
Working pressure (mTorr)	700	700	700	700

Table 2. Etching conditions of a-SiN:H, a-Si:H, n^+ a-Si:H and backside n^+ a-Si:H

Parameter	a-SiN:H, a-Si:H, n^+ a-Si:H	Backside n^+ a-Si:H
Gas	SF_6	SF_6
Flow rate (sccm)	20	20
r.f. power (W)	40	20
Substrate temperature (°C)	25	25
Working pressure (mTorr)	150	150
Etching time	18 min	14 sec

doped a-SiN:H thin films. HP-4156C was used to measure I-V, on/off ratio and transfer characteristics of the fabricated thin film transistor.

The field effect mobility in the saturation region μ_{sat} was calculated from Eq. (1) which is independent of V_{th} parameter.

$$I_d = C_i \mu_n W/(2L)(V_g - V_{th})^2 \quad (1)$$

C_i is the capacitance per unit area of the gate insulator and L/W (1:50) is the channel length/width ratio.

Results and Discussion

Figure 3 shows the drain current (I_D) versus drain voltage (V_D) characteristic of the TFT with various phosphorus doping concentrations in the a-SiN:H layer. At a fixed gate voltage of $V_G = 20$ V, the output drain current was increased with phosphine

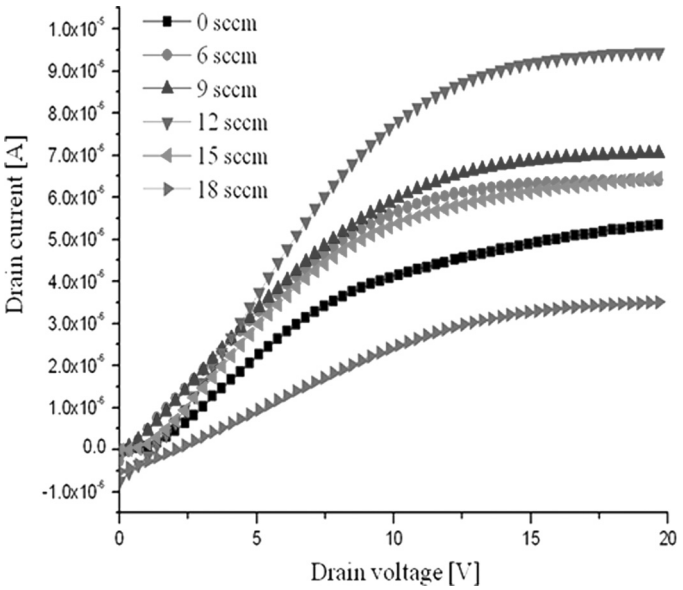

Figure 3. I_D-V_D characteristics of the inverted staggered a-Si:H TFT.

(PH_3 1% + H_2 99%) flow rate from 0 sccm to 12 sccm during deposition. However, the output current started to decrease as the phosphine flow rate increased to more than 12 sccm. This may result from the fact that the mobility increased with the phosphorus doing concentration until the phophine flow rate of 12 sccm due to increase of the charge carriers. However, it decreased since ion scattering would be dominate if the phophine flow rate is over 12 sccm.

Figure 4 shows the threshold voltages and the field-effect mobility with respect to the phosphorus concentration. The threshold voltages decreased from 5.1 V to 3.8 V with increasing the phosphine flow rates from 0 sccm to 12 sccm while the field effect mobility increased from 0.14 to 0.28 $cm^2/V \cdot s$ with increasing the phosphine flow rates from 0 sccm to 12 sccm.

Figure 5 shows the on/off current ratio characteristics of the TFTs with various doping concentrations. The range of on/off current ratio of the non-doped a-SiN:H layer and the phosphorus doped a-SiN:H layers (6, 9, 12, 15, 18 sccm) was between 1×10^4 and 1×10^6. As the phosphine flow rates increased from 0 sccm to 12 sccm the on/off current ratio increased upto 1×10^6. However, on/off current ratio decreased as the phosphine flow rate increased over 12 sccm.

Figure 6 shows that the surface roughness versus the phosphine flow rate in the SiNx layer. The surface roughness was measured with an atomic force microscope (AFM). The RMS of the surface roughness decreased from 1,878 nm to 649 nm with increasing the phosphine flow rates from 0 sccm to 12 sccm. However, the RMS of the surface roughness increased when phosphine flow rate was more than 12 sccm.

Figure 7 shows the three-dimensional AFM images of the surfaces deposited with various phosphine flow rates. The rough surface can cause a wide tail state and a high defect density, which deteriorates the TFT performance. According to Y. Kuo, an inadequate deposition condition, such as a high plasma power or a high

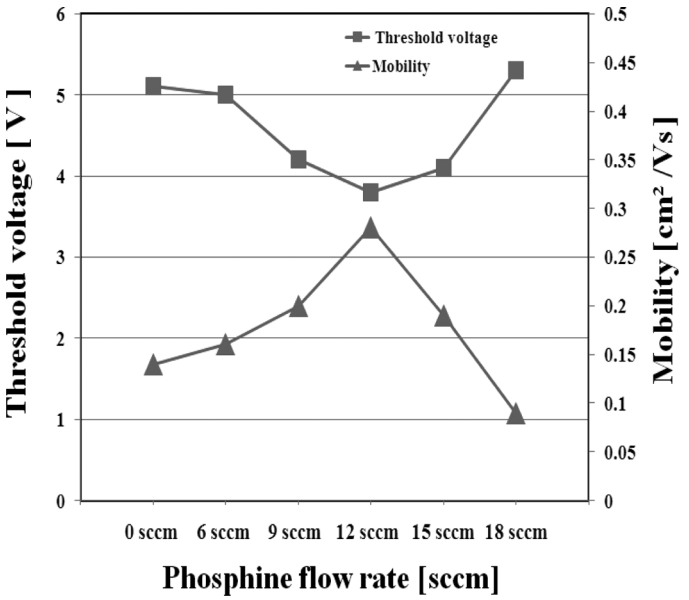

Figure 4. Threshold voltage and field effect mobility of the inverted staggered a-Si:H TFT.

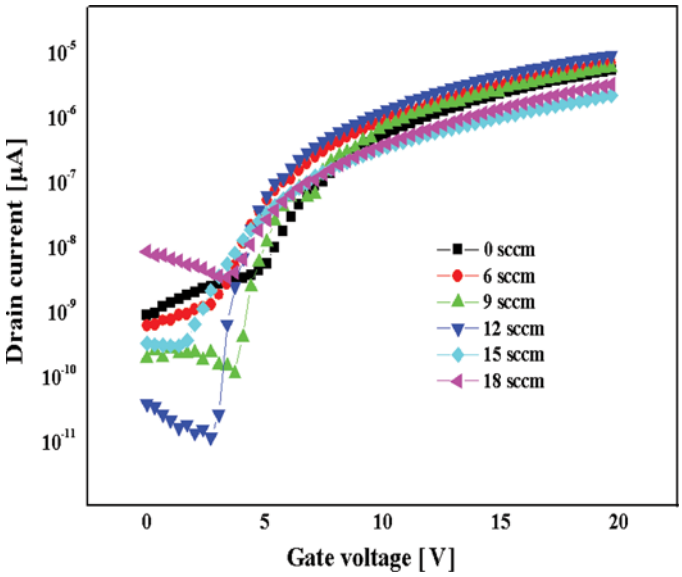

Figure 5. On/off current ratios of the inverted staggered a-Si:H TFT.

hydrogen concentration, could cause the surface roughness [6]. This measurement standards (data scale and data size) were 10 nm and 5 μm, respectively. In this study, the deposition condition becomes inappropriate as the phosphine flow rate was farther apart from 12 sccm.

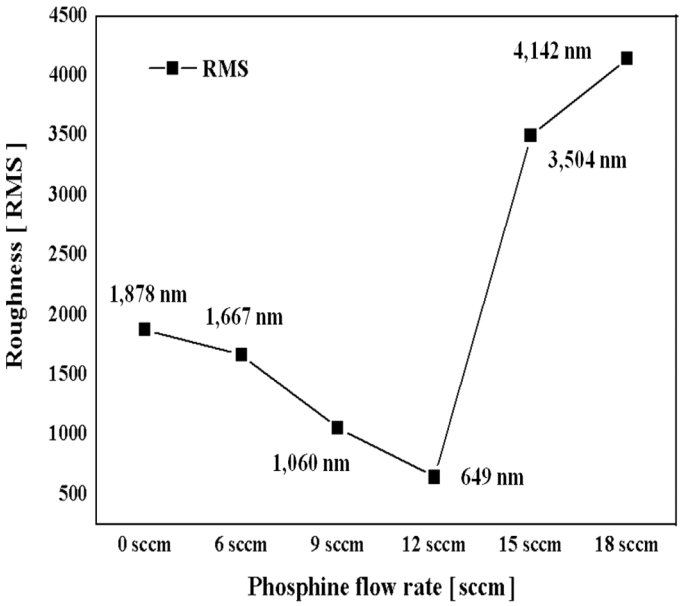

Figure 6. Surface roughness (RMS) of the a-SiN:H thin films.

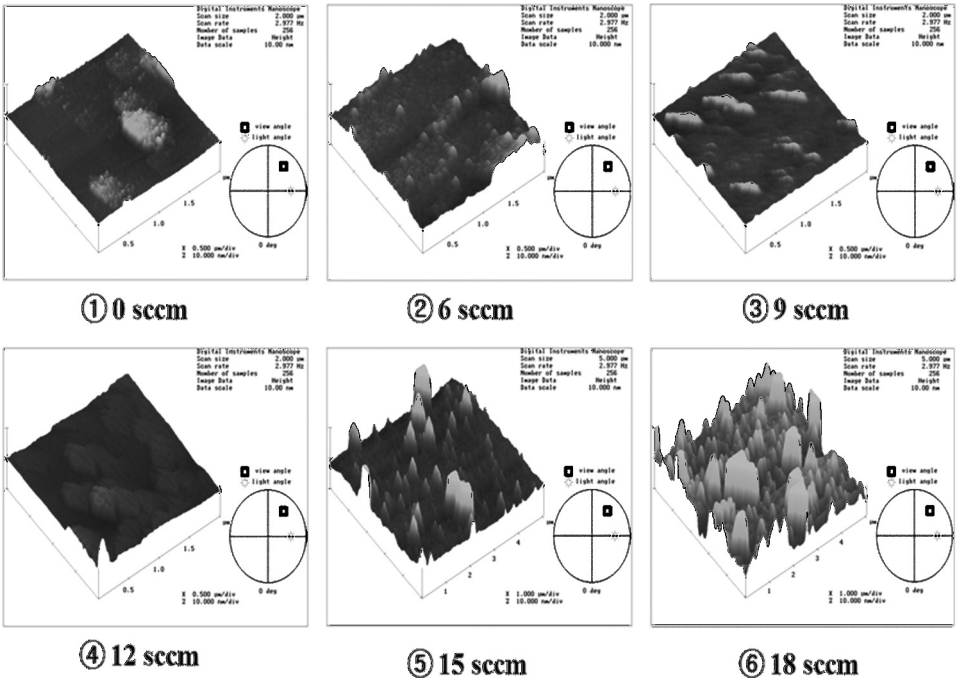

Figure 7. 3D (three-dimensional) AFM images of the a-SiN:H thin films.

Conclusions

This article has investigated the effect of phosphorus doping on the electron mobility of the TFTs. It has been found that the mobility was varied with the phosphorus doping concentrations.

Using this configuration, the high electron concentration in the channel can be achieved while retaining high mobility, since the a-Si:H channel region is spatially separated from the ionized impurities which provide the free carriers. But the mobility was decreased with increasing phosphine doping flow rate over 12 sccm. Because too much phosphorus doping within a-SiN:H thin film has a bad effect to the dielectric properties of a-SiN:H thin film. From the experimental results, the mobility, threshold and surface roughness at the a-SiN:H/a-Si:H interface were optimized at the phosphine flow rates of 12 sccm. The a-Si:H TFT at this phosphorus doping concentration showed higher mobility, lower threshold voltage and lower surface roughness. From the results the optimized device are significantly improved compared to the conventional (non-doped) a-Si:H TFTs.

Acknowledgments

This work was supported by the Regional Innovation Center Program (RIC) and the Brain Korea 21 (BK21), Republic of Korea.

References

[1] Sah, W. J., Lin, J. L., & Lee, S. C. (1991). *IEEE Trans. Electron Devices*, *38*, 676–678.
[2] Kobayashi, I., Ogawa, T., & Hotta, S. (1992). *Phys. Rev. Lett.*, *31*, 336.

[3] Kuo, Y. (1993). *Phys. Rev. Lett.*, *63*, 144.
[4] Jung, H. C., Park, K. M., Moon, K. H., Lee, T. Y., & Choi, S. Y. (2008). *The 12th Int. Symp. on ADMD*, *12*, 309–310.
[5] Kagan, C. R. (2003). *Thin-Film Transistors*, Marcel Dekker, Inc., 73–74.
[6] Kuo, Y. (1998). *Vacuum*, *51*, 741–745.